

Saad Anees

Associate Verification Engineer (ASIC/SOC/VIP)



Saad Anees



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EXPERIENCE

IMPARE | ASSOCIATE VERIFICATION ENGINEER

Jan 2023 – Present | Islamabad, Pakistan

- Provide RTL design and verification services
- Developed verification plans and executed them
- Develop verification test benches using SV/UVM
- Create and execute test cases to verify functionality
- Conduct coverage analysis and develop new test cases to target uncovered code and missing features
- Developed an AHB Verification IP based on UVM
- Developed UVM-based DV environments for USB 2.0

XELOGIX | INTERNEE

Aug 2021 – October 2021 | Islamabad, Pakistan

- Assisted in the design and analysis of electrical systems and components
- Monitored maintenance and inspection plans
- Collaborated with engineers on various engineering projects
- Participated in testing and troubleshooting electrical equipment and systems

PROJECTS

USB 2.0/VERIFICATION | SV/UVM

2023 - Present

- Created verification test plan
- Developed the DV environment
- Designed and implemented a scalable scoreboard that compared actual output against predicted data, ensuring design correctness.
- wrote test cases to validate functionality

UART RTL DESIGN/VERIFICATION | VERILOG/UVM

2023

- Designed and implemented a Universal Asynchronous Receiver-Transmitter (UART) using Register-Transfer Level (RTL) methodology. The project aimed to develop a robust and efficient communication interface for serial data transmission between digital devices
- Developed and executed a UVM-based test environment of the UART design

AHB VIP/DESIGN | SV/UVM

2023

- Developed an AHB Verification IP based on UVM
- The AHB-VIP Supports:
 - Non-sequential, Non-pipelined transfers
 - 8, 16, and 32-bit read and write transactions

SELF-DRIVING CAR (FYP) | PYTHON

2021 - 2022

- Designed a prototype self-driving car using Deep Neural Networks
- Implemented computer vision and machine learning techniques to detect lane lines and traffic signs.

SKILLS

PROGRAMMING

- Verilog/SystemVerilog
- UVM
- Python
- C/C++

EDA TOOLS

- Synopsys VCS/Verdi
- Synopsys Design Compiler
- Xilinx

PROTOCOLS

- USB 2.0
- UART
- AHB
- AXI

SOFTWARE TOOLS

- Git
- Implemented CI checks on GitHub to automate testing and ensure early detection of design issues.

EDUCATION

CAPITAL UNIVERSITY OF SCIENCE AND TECHNOLOGY (CUST)

BACHELORS IN ELECTRICAL ENGINEERING

Sep 2018 - July 2022 | Islamabad, PK

Cum. GPA: 3.62 / 4.0

PUNJAB GROUP OF COLLEGES

FSC. PRE-ENGINEERING

2016 - 2018 | Rawalpindi, PK

Board of Intermediate and Secondary Education (BISE)

Percentage : 80%